A' amd. 6

(b) gate array basic cells formed in an empty space of a predetermined cell row of the plurality of cells rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

A2

19. (Amended) A semicustom integrated circuit having a logic circuit area and at least one of megacell and megafunction on a single semiconductor chip, the logic circuit area comprising:

(a) a plurality of cell rows, in each row a plurality of standard cells are arranged, the standard cells being configured as rectangular pattern regions having a predetermined height, and different widths so that the standard cells include first and second type cells; and

(b) gate array basic cells formed in an empty space of the standard cells in predetermined cell row of the plurality of cell rows, each of the basic cells being configured as a rectangular pattern region having a height substantially identical to said predetermined height and a width equal to the width of the first type cell, said width of the basic cells not being equal to the width of the second type cell.

IN THE DRAWINGS

By way of a separate letter attached hereto, Applicants propose to amend Fig. 8 as indicated in red on the attached sheet. With the Examiner's approval, the changes will be incorporated into the formal drawings.